date of Patent No. 6,028,437 provides the required explanation particularly stating the basis upon which the applicants are prima facie entitled to the judgment.

With reference to the rejection of the claims under 35 U.S.C. 102(e) and 35 U.S.C. 103(a), it is apparent that the Potter patent either is or is not available as a reference in this application; it must be one or the other and cannot be both by elementary logic. If it is cited solely in rejection of claims under 35 U.S.C. 102(e) or 35 U.S.C. 103(a), then the Declarations filed November 6, 2001 and November 15, 2001 under 35 U.S.C. 1.131 remove Potter as a proper reference in this application under those sections of the statute. Accordingly, none of the rejections can comply with the requirements of 35 U.S.C. 102(e) or 103(a) since all art rejections are based entirely or partially on the Potter patent. On the other hand, if the examiner is of the opinion, as advanced by applicants and demonstrated in the REMARKS both hereinbelow and in the amendment filed November 6, 2001, that applicants cannot swear back of Potter due to claiming of the same invention as claimed by Potter, then it is incumbent upon the examiner to declare the interference and withdraw the rejection on prior art. It is readily apparent that the rejection on prior art is without merit in any event and this rejection is therefore respectfully traversed for reasons stated above.

In view of the above argument, it is clear that the section of the Office action under Declaration on page 2 thereof is without merit since the Potter reference is disqualified from use as prior art in this application in view of the Declarations filed under 37 C.F.R. 1.131, these Declarations now also being filed as Declarations under 37 C.F.R. 1.608(b).

With reference to the allegation under Interference on page 2 of the Office action in paragraph 4, it is respectfully submitted that each limitation of each claim copied for purposes of interference required to provoke an interference in this application has been read on the subject application in the Remarks presented in the amendment. Potter's claims are assumed at this time to be prima facie readable on Potter by the grant of the patent which is presumed to be valid. As long as one claim of Potter is copied and shown to be readable on the subject disclosure, an interference should be provoked.

As stated in the amendment filed November 6, 2001 claims 22 to 31 of this application are readable on the Potter patent No. 6,028,437. In that response, the necessary claims were read on the Potter patent and this will be repeated herein as well as for the claims not previously specifically shown to be readable on the subject disclosure.

Claim 22 above is the same as claim 1 of Potter except that the terms used in the subject application "interconnecting medium" have been used in place of the term --probe membrane-- and "medium surface" has been used in place of the term --probe membrane head--. This readability should be sufficient to provide a first count (claim 9 of the subject application can also be used as an additional or alternate count) for purposes of interference with all other claims coming under the count or counts. Claim 22, which is essentially the same as claim 1 of Potter except as noted above, is therefore readable on the subject disclosure as follows with the bracketed words being those used in Potter:

An apparatus adaptable for the testing of semiconductor devices comprising:

a package (110 of Fig. 1); and

an interconnecting medium (140) [probe membrane] contained within said package having electrical paths (171-173) adaptable for coupling to test circuitry,

wherein said interconnecting medium [probe membrane] includes a medium surface (top surface of 140 in Fig. 1b) [probe membrane head], a plurality of standoffs (13 of Fig. 3) affixed to said medium surface [probe membrane], and a plurality of probe tips (11 of Fig. 3) affixed to said medium surface [probe membrane head], said probe tips adaptable for making electrical contact with pads on said semiconductor device, wherein said probe tips are compliant bump probe tips.

Claim 9 is readable on Potter as follows:

9. An interconnecting layer for use in a semiconductor package which comprises;

(a) an electrically insulating layer (121 of Potter);

(b) electrically conductive paths on said layer (traces not shown but discussed at column 3, lines 45 to 57), each of said paths having first and second spaced apart regions thereon, said second spaced apart region of each of said paths having a compliant bump (122) having a height greater than all other structures on said layer; and

(c) a standoff (123) disposed on said layer and having a height above said layer and less than said bump.

With reference to the remaining claims of Potter, these claims would come in under the count, whether or not they can be made in the subject application. Accordingly, the interference should be declared just on the basis of the readability of claims 22 and 9 on the Potter patent. Under the interference Rules, additional claims can be added to come under the count in the Motion period.

With reference to claim 23, this claim is readable on the subject disclosure as follows:

said package (110) further comprising: a package base having an upper surface adapted (base of cavity 112) to receive said interconnecting medium (140), said medium having a medium lower surface (lower surface of 140);

a bonding layer interposed between said medium lower surface and said package base upper surface (120 and 135); and

a package lid (160) having a lower surface adapted to receive said semiconductor device, wherein said package lid is positioned above said package base.

With reference to claim 24, the claim is readable on the subject disclosure as follows:

said bonding layer (120 and 135) is comprised of an elastomeric material.

With reference to claim 25, the claim is readable on the subject disclosure as follows:

said semiconductor device is a die (130) having an upper surface, said upper surface fixed to said package lid lower surface by a bonding layer interposed therebetween (140 and 150).

With reference to claim 26, the claim is readable on the subject disclosure as follows:

said semiconductor device is a wafer (130) having an upper surface, said upper surface fixed to said package lid lower surface by a bonding layer interposed therebetween (140 and 150).

With reference to claims 27 and 28, these claims are readable on the subject disclosure as follows:

said bonding layer interposed between said die and said package lid lower surface is comprised of an elastomeric material (page 9, line 11).

With reference to claim 29, this claim is readable on the subject disclosure as follows:

the compliant bump probe tips are comprised of a solid material (see, for example, Patent No. 5,508,228 cited at page 11, line 15).

With reference to claim 30, this claim is readable on the subject disclosure as follows:

An apparatus adaptable for the testing of semiconductor devices comprising:

a package (110 of Fig. 1), wherein said package has a package lid (160) having a lower surface adapted for receiving said semiconductor device, said semiconductor device (130) having an upper surface, and a package base having an upper surface (112);

an interconnecting medium (140) contained within said package, wherein said interconnecting medium has electrical paths (171, 172, 173) adaptable for coupling to test circuitry, said medium including a medium surface, said medium surface having a plurality of probe tips (11) affixed thereto, a plurality of standoffs (13) affixed thereto, and a lower surface, wherein said probe tips are adaptable for making electrical contact with pads (135) on said semiconductor device (130) and are compliant bump probe tips (sentence bridging pages 9 and 10);

a bonding layer (120, 135) comprising an elastomeric material (page 9, line 11) interposed between said package lid lower surface and said semiconductor device upper surface; and

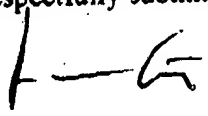
a bond layer (140, 150) comprising an elastomeric material interposed between said interconnecting medium lower surface and said package base upper surface, said package base being adapted for receiving said interconnecting medium.

With reference to claim 31, this claim is readable on the subject disclosure as follows.

the compliant bump probe tips are comprised of a solid material (see, for example, Patent No. 5,508,228 cited at page 11, line 15).

In view of the above and the Declarations previously filed, reconsideration and institution of an interference are respectfully requested.

Respectfully submitted,



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30. An apparatus adaptable for the testing of semiconductor devices comprising:

a package, wherein said package has a package lid having a lower surface adapted for receiving said semiconductor device, said semiconductor device having an upper surface, and a package base having an upper surface;

an interconnecting medium contained within said package, wherein said interconnecting medium has electrical paths adaptable for coupling to test circuitry, said medium including a medium surface, said medium surface having a plurality of probe tips affixed thereto, a plurality of standoffs affixed thereto, and a lower surface, wherein said probe tips are adaptable for making electrical contact with pads on said semiconductor device and are compliant bump probe tips;

a bonding layer comprising an elastomeric material interposed between said package lid lower surface and said semiconductor device upper surface; and

a bond layer comprising an elastomeric material interposed between said interconnecting medium lower surface and said package base upper surface, said package base being adapted for receiving said interconnecting medium.